Review Paper on Efficient VLSI Architecture for Discrete Cosine Transform

Sonam Nema¹, Adesh Gour²
PG Student¹, HOD & Professor²
Department of Electronics & Communication Engineering
SAM College of Engineering & Technology

Abstract—Low-power design is one of the most important challenges to maximize battery life in portable devices and to save the energy during system operation. Discrete Cosine Transform (DCT) is widely used in image and video compression standards. In this paper, we review on a low-power DCT (Discrete Cosine Transform) architecture using varies techniques. Discrete Cosine Transform (DCT) is one of the most popular lossy techniques used today in video compression schemes. Several algorithms have been proposed to implement the DCT. Loeffler (1989) has given a new class of 1D-DCT using just 11 multiplications and 29 additions. To implement such an algorithm, one or more multipliers have to be integrated. This requires a high silicon occupation area. Arithmetic distribution is widely used for such algorithms. The coding for reconfigurable 8 point DCT has been done using VHDL under Xilinx platform.

Keywords: - Discrete Cosine Transform (DCT), Inverse discrete Cosine Transform (IDCT), VHDL

I. INTRODUCTION

The rapid growth of multimedia services running on portable applications demands low power and high quality implementation of complex signal processing algorithms. The applications of multimedia systems involve image and video processing and it should be implemented with low cost and low power because of limited battery lifetime. Many papers have been published on reducing power dissipation of image and video applications, especially low power design of discrete cosine transform [1]. DCT is a computation intensive operation in image and video compression. It is used in image and video compression standards such as JPEG [2], MPEG, H.263 [3] and H.264. The direct implementation of DCT requires large number of multipliers and adders. Many previous works focused on Distributed Arithmetic (DA) based DCT & multiple constant multiplications [4]. To reduce the power consumption Distributed Arithmetic (DA) is used without multiplier [5]. DCT implementation using distributed arithmetic [DA] includes several advantages such as area reduction and high speed performance. High speed can be achieved by using conventional DA implementation by pre-computing possible values and storing it in ROM. But ROM based DA has the disadvantage of redundancy which is introduced to accommodate all possible combinations of bit patterns of input signals. A regular and simple DCT architecture can be obtained by using bit serial DA based approach. MCM based DCT can be implemented with a smaller number of shifts and add operations.

The Discrete Cosine Transform (DCT) is a Fourier-like transform, which was developed by Ahmed, Natarajan and Rao in 1974. It has become one of the most widely used transform techniques in digital signal processing. The DCT is one of the computationally intensive transforms which require many multiplications and additions [1], while the Fourier Transform represents a signal as the mixture of sine and cosine, the Cosine Transform performs only the cosine-series expansion. The purpose of DCT is to perform de-correlation of the input signal and to present the output in the frequency domain. The DCT is known for its high “energy compaction” property, meaning that the transformed signal can be easily analyzed using few low-frequency components [4]. It turns out to be that the DCT is a reasonable balance of optimality of the input de-correlation (approaching the Karhunen-Loève transform) and the computational complexity. This fact made it widely used in digital signal processing [2].

The entire fast algorithm still require floating point multiplication which is slow in both hardware and software implementation. To achieve faster implantation, coefficients can be scaled and approximated by integer such as floating point multiplication can be replaced by integer multiplication [6]. This can be done by rounding floating point value to integer value by multiplying floating point value. Where can be any integer number? This is called as fixed point arithmetic. The resulting algorithms are much faster than the original version and therefore have wide practical applications.

II. LITERATURE REVIEW

Mansi Mane et al. [1], CORDIC or CO-ordinate Rotation Digital Computer is a fast, simple, coherent and powerful algorithm which is used for diversified Digital Signal Processing applications. In pursuance of speed and accuracy requirements of today’s applications, we put forward variable iterations CORDIC algorithm. In this algorithm, to boost
speed we can lessen number of iterations in CORDIC algorithm for specific accuracy. This enhances efficiency of conventional CORDIC algorithm which we have used to compute Discrete Cosine Transform for image processing. One Dimensional Discrete Cosine Transform is implemented by using only 6 CORDIC blocks which needs only 6 multipliers. Because of the simplicity in hardware speed of image processing on FPGA is raised. Further increase in speed can be achieved by concurrently processing number of macro-blocks of an image on FPGA.

The proposed CORDIC based 2D DCT architecture is simulated using Modelsim and the experimental results show that our reconfigurable DCT achieves power savings with improved image quality. All the computations in DCT are not equally important in generating the frequency domain output. Considering the important difference in the DCT coefficients the number of CORDIC iterations can be dynamically changed to reduce the power of consumption with improved image quality.

III. DISCRETE COSINE TRANSFORM

A discrete cosine transform (DCT) expresses a finite sequence of data points in terms of a sum of cosine functions oscillating at different frequencies. DCTs are important to numerous applications in science and engineering, from lossy compression of audio (e.g. MP3) and images (e.g. JPEG) (where small high-frequency components can be discarded) to spectral methods for the numerical solution of partial differential equations. The use of cosine rather than sine functions is critical for compression, since it turns out (as described below) that fewer cosine functions are needed to approximate a typical signal, whereas for differential equations the cosines express a particular choice of boundary conditions.

DCT output

\[
\begin{align*}
F(0) &= 0.5(f(0) + f(1) + f(2) + f(3) + f(4) + f(5) + f(6) + f(7))\cos\frac{\pi}{4} \\
F(1) &= 0.5\left[(f(0) - f(7))\cos\frac{\pi}{16} - \{f(1) - f(6)\}\cos\frac{3\pi}{16} - \{f(2) - f(5)\}\cos\frac{5\pi}{16} + \{f(3) + f(4)\}\cos\frac{7\pi}{16}\right] \\
F(2) &= 0.5\left[(f(0) - f(3) - f(4) + f(7))\cos\frac{2\pi}{16} + \{f(1) - f(2) - f(5) + f(6)\}\cos\frac{6\pi}{16}\right]
\end{align*}
\]

Figure 1: 8-point Discrete Cosine Transform

Hyeonuk Jeong et al. [2], Low-power design is one of the most important challenges to maximize battery life in portable devices and to save the energy during system operation. In this paper, we propose a low-power DCT (Discrete Cosine Transform) architecture using a modified multiplier-less CORDIC (Coordinate Rotation Digital Computer) arithmetic. The switching power consumption is reduced during DCT: the proposed architecture does not perform arithmetic operations of unnecessary bits during the CORDIC calculations. The experiment results show that we can reduce up to 26.1% power dissipation without compromise of the final DCT results. Also, the speed of the proposed architecture is increased about 10%. The proposed low-power DCT architecture can be applied to consumer electronics and portable multimedia systems requiring high throughput and low-power.

Esakkirajan G et al. [3], CORDIC or CO-ordinate Rotation Digital Computer is a fast, simple, efficient and powerful algorithm used in Digital Signal Processing applications. In this paper, we extend the methodology for designing a low-power area-efficient DCT for image compression using only shift registers, and adders! Subtractors and special interconnections. Through hardware synthesis we proved that shift and add based DCT computation is efficient one over conventional multiplier based approach and finally accuracy was measured by comparing PSNR value of reconstructed image with original image using MATLAB.

E. Jebamalar Leavline et al. [4], Discrete Cosine Transform (DCT) is widely used in image and video compression standards. This paper presents low-power co-ordinate rotation digital computer (CORDIC) based reconfigurable architecture for discrete cosine transform (DCT).
\[ F(3) = 0.5 \left\{ (f(0) - f(7)) \cos \frac{3\pi}{16} + (f(6) - f(1)) \cos \frac{7\pi}{16} + (f(5) - f(2)) \cos \frac{\pi}{16} + (f(4) + f(3)) \cos \frac{5\pi}{16} \right\} \]

\[ F(4) = 0.5 \left\{ (f(0) + f(3) + f(4) + f(7)) - (f(1) - f(2) - f(5) - f(6)) \cos \frac{\pi}{4} \right\} \]

\[ F(5) = 0.5 \left\{ (f(0) - f(7)) \cos \frac{5\pi}{16} + (f(6) - f(1)) \cos \frac{\pi}{16} + (f(2) - f(5)) \cos \frac{7\pi}{16} + (f(3) + f(4)) \cos \frac{3\pi}{16} \right\} \]

\[ F(6) = 0.5 \left\{ (f(0) - f(3) - f(4) + f(7)) \cos \frac{6\pi}{16} - (f(1) - f(2) - f(5) + f(6)) \cos \frac{2\pi}{16} \right\} \]

\[ F(7) = 0.5 \left\{ (f(0) - f(7)) \cos \frac{7\pi}{16} + (f(6) - f(1)) \cos \frac{5\pi}{16} + (f(2) - f(5)) \cos \frac{3\pi}{16} + (f(4) + f(3)) \cos \frac{\pi}{16} \right\} \]

IV. SIMULATION RESULT

All the designing and experiment regarding algorithm that we have mentioned in this paper is being developed on Xilinx 14.1i updated version. Xilinx 9.2i has couple of the striking features such as low memory requirement, fast debugging, and low cost. The latest release of ISE® (Integrated Software Environment) design tool provides the low memory requirement approximate 27 percentage low.

![Figure 2: RTL View of 8-point Discrete Cosine Transform](image)

ISE 14.1i that provides advanced tools like smart compile technology with better usage of their computing hardware provides faster timing closure and higher quality of results for a better time to designing solution. ISE 14.1i Xilinx tools permits greater flexibility for designs which leverage embedded processors. Show the Spartan-2 device family result in 8-point DCT, but 8-point DCT 731% percent used in this device so we are going to Spartan-2 to vertex-2p device family.

V. CONCLUSION

In literature survey we found that CORDIC based DCT algorithm is the best algorithm in the existing algorithm. So we are implementation to CORDIC based DCT algorithm in this paper. The performance evaluation of the various sub modules are carried out using Xilinx 14.1 ISE Simulator and it was found that the circuits designed using DCT logic showed a reduced delay and power. As a future work more arithmetic and logical function can be used.
REFERENCES


